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Superlattice-like $Ga_{40}Sb_{60}$/Sb films with ultra-high speed and low power for phase change memory application

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Abstract Superlattice-like (SLL) $Ga_{40}Sb_{60}$/Sb (GSS) is proposed for its ultra-high speed, low power for phase change application. The excellent properties derives from the properly designed SLL structure of Sb layers with high speed and low crystallization temperature (T_c) inserting high T_c $Ga_{40}Sb_{60}$. Appropriate T_c $\sim$ 220 °C and ultra-long data retention (151 °C for 10 years) is obtained in the SLL $[Ga_{40}Sb_{60}(5\ nm)/Sb(4\ nm)]_5$ thin films. X-ray diffraction analysis shows that only Sb phase exists in the SLL GSS thin films and the low surface roughness is confirmed by AFM measurement. Moreover, the phase change memory devices based on $Ge_2Sb_2Te_5$ (GST) and SLL $[Ga_{40}Sb_{60}(5\ nm)/Sb(4\ nm)]_5$ thin films were fabricated and the set and reset operation was studied. The current–voltage measurement for set operations shows the threshold switching voltage (2.0 V) is smaller than the GST (4.4 V). The resistance–voltage tests indicate the reversible phase change could be realized by a pulse as short as 10 ns and the reset power of the $[Ga_{40}Sb_{60}(5\ nm)/Sb(4\ nm)]_5$ cell calculated as 2.3×10^{-11} J is 6.5 times lower than the GST cell 1.5×10^{-10} J.

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1 Introduction

Phase change memory (PCM), proposed by S. Ovshinsky in the 1960s, has been considered as one of the most promising nonvolatile memories because of its excellent properties such as high speed, low power consumption, perfect data retention capability and fabrication compatibility with complementary metal–oxide–semiconductor (CMOS) technology [1–3]. Recently, many efforts have been made to find suitable materials in PCM application. Te-based chalcogenide alloys, especially the $Ge_2Sb_2Te_5$ (GST), are generally considered to be the prototype materials for application in PCM [4, 5]. However, the Te element is harmful to semiconductor techniques due to its volatilization and the presence of Te will lead to the phase-segregation after cycling and insufficient data retention [6, 7]. In addition, the PCM device based on GST material is difficult to have an entire operating window when the width of the voltage pulse is shorter than 100 ns, which is insufficient to satisfy the requirement of dynamic random access memory (DRAM; 10 ns) [8]. To overcome these drawbacks and explore novel phase change materials, Te-free and Sb-rich alloys such as GaSb [9], GeSb [10], SnSb [11], have been proposed as alternatives due to their very short crystallization times (<15 ns).

In general, a material with a fast phase speed is not stable [12]. In order to solve this contradiction, a type of artificial structure called "superlattice-like" (SLL) structure has been designed to maintain the high phase change speed and good stability. In the SLL structure, one phase change material has a high crystallization speed and another has relatively low crystallization speed but high stability. Moreover, the cells of PCM device with the SLL structure exhibit a lower operation power and fast read-

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write speed due to their lower thermal conductivity compared to monolayer materials [12–14].

Gallium antimonide (GaSb) is a direct band gap material which can be used for PCM application [15]. Especially in Ga_xSb_{100-x} alloys, the crystallization temperature (T_c) could be tuned by changing the concentration of Sb [6]. $Ga_{40}Sb_{60}$ is a material with high T_c and the Sb is the material with fastest phase change speed but low T_c. In this work, we propose SLL $Ga_{40}Sb_{60}$/Sb (GSS) thin films. The electrical, thermal and structural properties were investigated in detail.

2 Experimental

In this work, the terminology $[Ga_{40}Sb_{60}(5\ nm)Sb(4\ nm)]_5$ indicates the SLL structure with a period of 5 nm $Ga_{40}Sb_{60}$/4 nm Sb and five cycles. The others can be deduced by analogy. The SLL $Ga_{40}Sb_{60}$/Sb (GSS) thin films of 50 nm thickness were deposited on SiO_2/Si (100) wafers with different layer thickness ratios of $Ga_{40}Sb_{60}$:Sb by magnetron sputtering the $Ga_{40}Sb_{60}$ and Sb target at room temperature. The base pressure in the deposition chamber was 2×10^{-4} Pa. Sputtering was performed under the Ar gas pressure of 0.3 Pa, the flow of 30 SCCM, and the power of 30 W. The thickness of each layer was controlled by deposition time. To ensure the uniformity of deposition, the substrate holder was rotated at an autorotation speed of 20 rpm. Before the growth of the samples, $Ga_{40}Sb_{60}$ and Sb deposition rates were estimated by measure the thickness of corresponding single layer target by Field Emission Scanning Electron Microscope (FESEM).

In situ temperature-dependent resistance (R–T) was performed using a two-point-probe setup to obtain the crystallization temperature by a TP 95 temperature controller (Linkam Scientific Instruments Ltd. Surry, UK). The samples were kept at different temperature for isothermal R–T measurements to estimate the data retention time and the activation energy for crystallization (E_a) by the Arrhenius equation. The optical band gap (E_{op}) was derived from the transmittance spectra in the wavelength range from 900 to 2000 nm. The crystalline structures of the films were analyzed by X-ray diffraction (XRD). The surface morphology of the films was examined by atomic force microcopy (AFM, FM-Nanoview 1000). The PCM devices based on the $[Ga_{40}Sb_{60}(5\ nm)/Sb(4\ nm)]_5$ thin film with a tungsten heating electrode of 260 nm diameter were fabricated by 0.18 μm CMOS technology. Between the GSS film and the top electrode, a 20 nm thick TiN film was deposited by direct current magnetron sputtering. Resistance–voltage (R–V) measurements were conducted using a Keithley 2400 semiconductor parameter analyzer and an Agilent 81104A programmable pulse generator.

3 Results and discussion

Relationships between resistance and temperature of the SLL GSS thin films and monolayer $Ga_{40}Sb_{60}$ thin film are shown in Fig. 1a. Due to thermally assisted trap-limited conduction, the resistance of all the thin films initial decreased slowly as the temperature increased. Then a rapid drop appears which is defined as the crystallization temperature (T_c). Figure 1 shows that T_c is dependent on the thickness ratio between the $Ga_{40}Sb_{60}$ and Sb layer. With increasing relative thickness of Sb, the T_c decrease from the 340 °C of pure $Ga_{40}Sb_{60}$ to 105 °C of $[Ga_{40}Sb_{60}(5\ nm)/Sb(10\ nm)]_3$. Lu et al. [6] and Putero et al. [9] have studied the crystallization behavior of Ga-Sb alloys, indicating that the T_c shifted to lower temperature with the increasing concentration of Sb. Thus, the result of our work can be attributed to the increasing concentration of Sb and the lower T_c of amorphous Sb layer. It is well known that the T_c of the phase-change materials is the key factor for practical application because PCM devices must have good trade-off between high thermal stability (high T_c) and fast crystallization speed (generally low T_c). Therefore, it is very valuable that a suitable T_c would be tuned simply by the change in the thickness ratio between the $Ga_{40}Sb_{60}$ and Sb. The $[Ga_{40}Sb_{60}(5\ nm)/Sb(4\ nm)]_5$ with the appropriate T_c (220 °C) higher than GST (140 °C) [16] could be regarded as the optimal film for the application in PCM.

The optical band gap (E_{op}) can be calculate form the transmittance spectra by the absorption coefficient and photon energy, which can be described as [17]

$$\alpha h\upsilon = C\left(h\upsilon - E_{op}\right)^n \quad (1)$$

where $\alpha = -(\ln T)/d$ (T is the transmittance and d is the depth of the thin film); $h\upsilon$ is the photon energy; n is an appropriate selected index (for the indirect amorphous chalcogenide semiconductor, the value of n is 2) [18]. The value of E_{op} is determined from the intercept on the energy axis with zero absorbance. As shown in Fig. 1b, it is apparently that the optical band gap significantly decreases with SLL structure of inserting of Sb layer. It is considered that the decrease of E_{op} is due to the presence of Sb layer (low E_{op}). Therefore, we believe that the decrease of E_{op} is the main reason for explaining the T_c decrease and amorphous resistance decrease in SLL structure.

Data retention capability of films is vital for PCM devices, which can be evaluated by extrapolation of the isothermal Arrhenius plot. With the thermal activation, the plot of logarithm failure time versus $1/k_bT$, which fit a linear Arrhenius relationship, defined as Eq. (2) [19]

$$t = \tau_0 \exp[E_a/K_bT] \quad (2)$$

where t, τ_0, k_b, T are the failure time, the pre-exponential factor depending on the materials' properties, Boltzmann

constant, and absolute temperature, respectively. Figure 2a illustrate the dependence of normalized resistivity on time for $[Ga_{40}Sb_{60}(5\ nm)/Sb(4\ nm)]_5$ film measured at different specified temperature. The failure time is defined as the time when the resistance decreased to a half of its initial value which can characterize the data retention. Figure 2a shows the failure time decreases obviously with increasing the annealing temperature.

The fitted line base on the failure time versus reciprocal temperature ($1/k_bT$) was plotted in Fig. 2b. The activation energy E_a of SLL GSS films obtained from the slope of the plot. Increasing Sb relative thickness, the E_a of the GSS films decrease from the 3.73 eV of $[Ga_{40}Sb_{60}(5\ nm)/Sb(3\ nm)]_6$ to 0.41 eV of $[Ga_{40}Sb_{60}(5\ nm)/Sb(10\ nm)]_3$. Accordingly, the temperature of 10 years lifetime decrease from 221 to −33 °C. The result indicates that the excellent thermal stability of SLL GSS thin films change into sudden worse reliability by increasing the Sb relative thickness. To compete with NOR-Flash memory, the data retention of 10 year for PCRAM at temperature should be higher than 125 °C [20]. From this perspective, PCM using GST, which have 10 year retention at 80–125 °C, cannot satisfy the requirement of consumer appliances and automotive systems. In our work, as shown in Fig. 2b, the data retention of 10 years can be manipulated in GSS SLL system. Especially, the SLL $[Ga_{40}Sb_{60}(5\ nm)/Sb(4\ nm)]_5$ thin films process data retention of 151 °C meaning longer data lifetime than GST, meeting the application of PCM devices.

The crystalline structures of films were characterized by XRD after annealing in N_2 atmosphere for 5 min in Fig. 3. As shown in Fig. 3, only the single hexagonal phase of Sb (PDF#35-0732) was observed in thin films. This can be attributed to the large of the Sb/Ga molar ratio in the SLL GSS films, leading to rapid crystallization of Sb [21]. Moreover, Fig. 3a indicates that SLL structure incorporating Sb layer can significantly decrease the T_c, which is accordance with the R–T measurement. Figure 3b shows

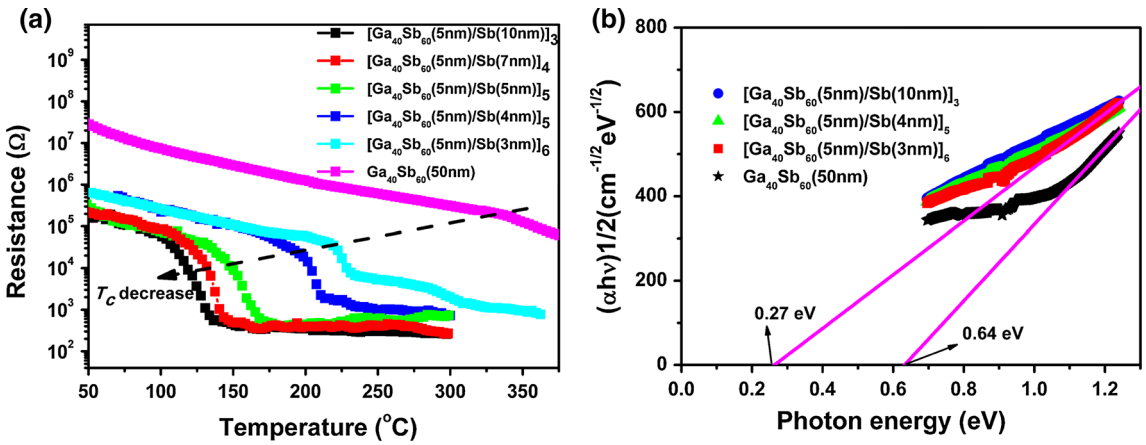

Fig. 1 **a** Resistance as a function of temperature for $Ga_{40}Sb_{60}$ and SLL $Ga_{40}Sb_{60}$/Sb thin films at a heating rate of 10 °C min^{-1}. **b** Plots of $(\alpha h\nu)^{1/2}$ versus hν for amorphous SLL $Ga_{40}Sb_{60}$/Sb thin films

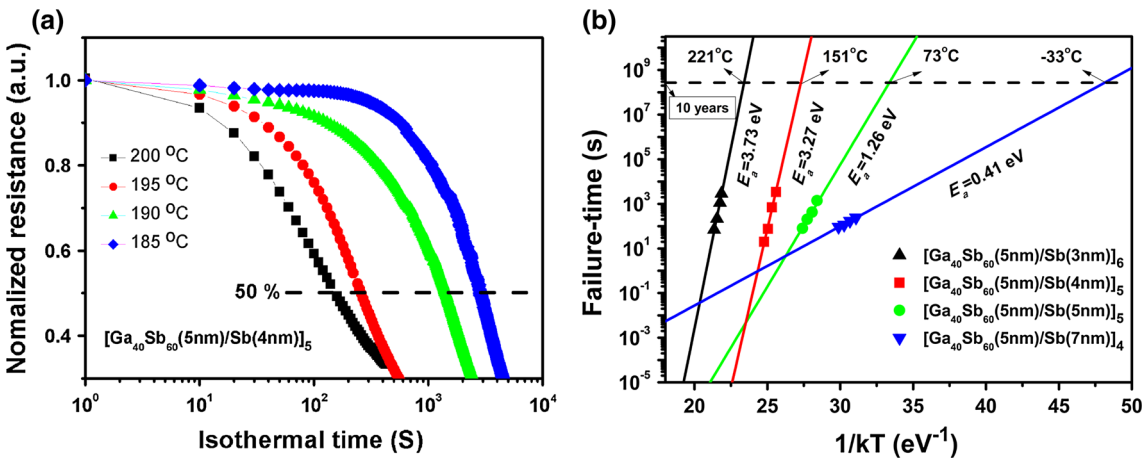

Fig. 2 **a** Normalized resistance of $[Ga_{40}Sb_{60}(5\ nm)/Sb(4\ nm)]_5$ thin film as a function of annealing time at various temperature. **b** Plots of failure time as a function of reciprocal temperature for SLL $Ga_{40}Sb_{60}$/Sb thin films

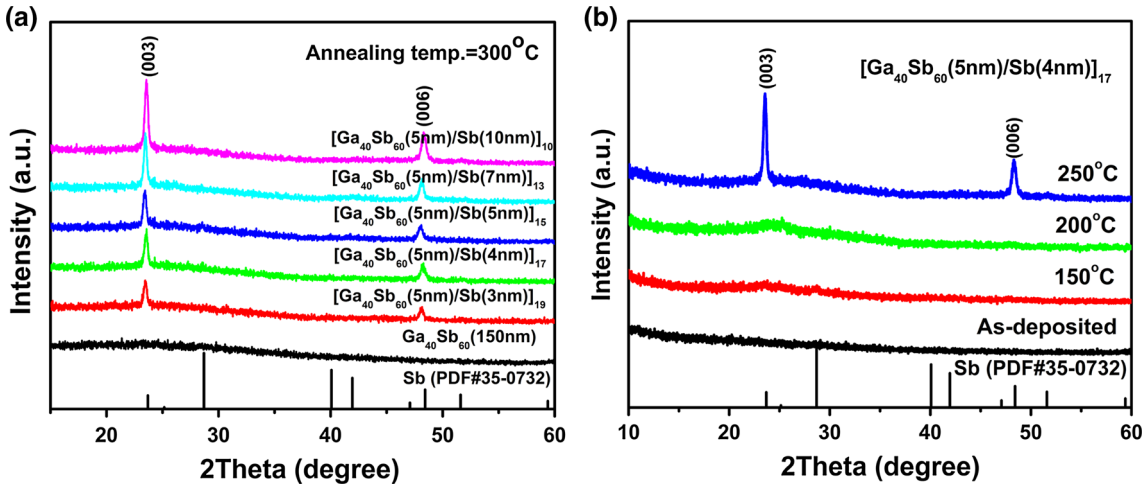

Fig. 3 **a** XRD patterns of $Ga_{40}Sb_{60}$(150 nm) and $[Ga_{40}Sb_{60}$(5 nm)/Sb(4 nm)$]_{17}$ thin films annealed at 300 °C for 5 min in Ar atmosphere. **b** XRD patterns of $[Ga_{40}Sb_{60}$(5 nm)/Sb(4 nm)$]_{17}$ films annealed at different temperature for 5 min in Ar atmosphere

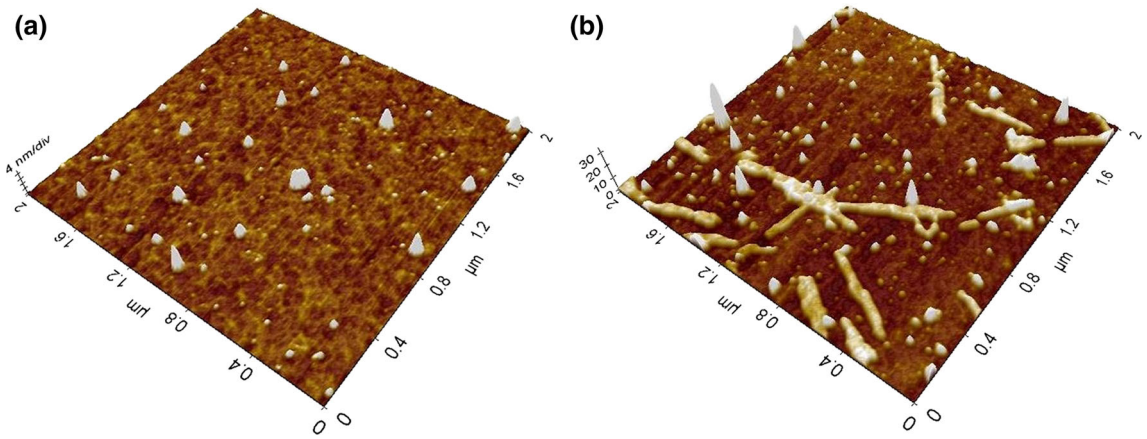

Fig. 4 AFM micrographs for $[Ga_{40}Sb_{60}$(5 nm)/Sb(4 nm)$]_5$ films (**a**) as-deposited (**b**) annealed at 250 °C for 5 min in Ar atmosphere

that the $[Ga_{40}Sb_{60}$(5 nm)/Sb(4 nm)$]_{17}$ film maintained amorphous structure for annealing temperature up to 200 °C. As the annealing temperature further increase from 200 °C to 250 °C, the crystallization peaks emerged obviously which can be assigned to phase transition. In general, the crystallization temperature is increased with decreasing the film thickness [22, 23]. In our work, the thickness of $[Ga_{40}Sb_{60}$(5 nm)/Sb(4 nm)$]_{17}$ thin film is bigger than the thickness of $[Ga_{40}Sb_{60}$(5 nm)/Sb(4 nm)$]_5$ thin film, which indicates the crystallization temperature of the $[Ga_{40}Sb_{60}$(5 nm)/Sb(4 nm)$]_5$ thin film will be higher than 200 °C. Thus, Fig. 3b shows that the $[Ga_{40}Sb_{60}$(5 nm)/Sb(4 nm)$]_{17}$ thin film can keep a stable amorphous state at temperature of 200 °C revealing the $[Ga_{40}Sb_{60}$(5 nm)/Sb(4 nm)$]_5$ would also process excellent thermal reliability for PCM application.

Film surface roughness is extremely important for device performance, since electrical properties depend on not only a well-defined microstructure but also quality of the electrode-film interface [24, 25]. The AFM image of $[Ga_{40}Sb_{60}$(5 nm)/Sb(4 nm)$]_5$ film before and after annealing are presented in Fig. 4. As shown in Fig. 4a, the root mean square (RMS) roughness calculated from the AFM images of as-deposited was 0.321 nm, which was smaller than the annealed SLL film of 0.931 nm. This result indicates the crystallization behavior will increase the film surface roughness. Compared with other results, such as Sn_2Se_3 [26], Sb_2Te_3 [24], the films of SLL GSS have relatively low RMS value, meaning excellent surface roughness for devices performance.

In order to test and verify the properties of SLL GSS films for PCM application, it is very necessary to observe the characteristic of PCM cells. The inset of Fig. 5a, shows the schematic of PCM cell device. For comparison, the GST-based PCM cells were also synthesized. Figure 5 shows the typical current–voltage (I–V) and resistance–

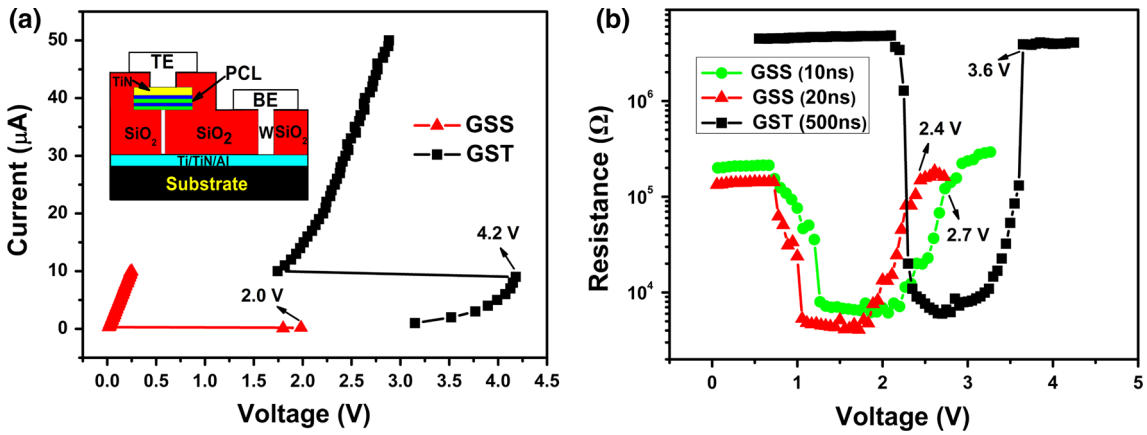

Fig. 5 **a** I–V characteristics of the cell devices based on GST and $[Ga_{40}Sb_{60}(5\ nm)/Sb(4\ nm)]_5$ thin films. The *inset* shows the schematic of PCM cell device; **b** R–V curves of the cell devices for GST and $[Ga_{40}Sb_{60}(5\ nm)/Sb(4\ nm)]_5$ thin films

voltage (R–V) curves of the devices. The I–V curve for SET operations, in Fig. 5a, is associated with the phase transition process from high resistance state (amorphous) to a low resistance state (crystalline). As shown in Fig. 5a, the threshold switching voltage (2.0 V) is smaller than the GST (4.2 V), also smaller than the $Ga_{14}Sb_{86}$-based cell (2.6 V) [27], which indicate less power consumption in SET process_ENREF_23. The R–V curves for reset operations, shown in Fig. 5b, are characterized when the programming voltage pulses applied to the cell. The reversible phase change could be realized by a pulse as short as 10 ns, indicating fast transformation speed of $[Ga_{40}Sb_{60}(5\ nm)/Sb(4\ nm)]_5$ thin film compared with the GST with 500 ns. In addition, the RESET voltage of $[Ga_{40}Sb_{60}(5\ nm)/Sb(4\ nm)]_5$ film (2.7 V at 10 ns) is smaller than the GST (3.6 V at 500 ns). The energy necessary for the RESET operation [28] is estimated $E_{reset} = V_{reset}^2/R_{reset} \times t_{reset}$. More importantly, the RESET power of the $[Ga_{40}Sb_{60}(5\ nm)/Sb(4\ nm)]_5$ cell is calculated as 2.3×10^{-11} J, which is 6.5 times lower than the GST cell 1.5×10^{-10} J.

4 Conclusion

In summary, superlattice-like (SLL) $Ga_{40}Sb_{60}$/Sb (GSS) thin films with different thickness of Sb layers were prepared by radio-frequency magnetron sputtering system. By inserting Sb layers, the suitable crystallization temperature (T_c) can be tuned simply by varying the thickness ratio of $Ga_{40}Sb_{60}$ and Sb layers. With the $T_c \sim 220$ °C and activation energy E_a of 3.27 eV, the SLL $[Ga_{40}Sb_{60}(5\ nm)/Sb(4\ nm)]_5$ have an ultra-long data retention, which is characterized by the temperature for ten years data retention at 151 °C larger than $Ge_2Sb_2Te_5$ (GST) (<120 °C). In addition, the XRD diffraction analyses demonstrated that the change of phase structure of GSS films with different annealing temperature. The surface roughness, with RMS 0.321 nm as-deposited film, was evaluated with AFM indicating the good film surface roughness for devices performance. The PCM cell devices based on GST and SLL $[Ga_{40}Sb_{60}(5\ nm)/Sb(4\ nm)]_5$ film were fabricated and the set and reset operation was studied. The results indicate the cell base SLL $[Ga_{40}Sb_{60}(5\ nm)/Sb(4\ nm)]_5$ film has faster speed and lower operation power consumption than GST-based cell.

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References

1. D. Loke, T.H. Lee, W.J. Wang, L.P. Shi, R. Zhao, Y.C. Yeo, T.C. Chong, S.R. Elliott, Science **336**, 1566–1569 (2012)
2. J. Tauc, R. Grigorovici, A. Vancu, Phys. Status Solidi B **15**, 627–637 (1966)
3. C. Peng, F. Rao, L. Wu, Z. Song, Y. Gu, D. Zhou, H. Song, P. Yang, J. Chu, Acta Mater. **74**, 49–57 (2014)
4. D. Ielmini, A.L. Lacaita, Mater. Today **14**, 600–607 (2011)
5. R.E. Simpson, M. Krbal, P. Fons, A.V. Kolobov, J. Tominaga, T. Uruga, H. Tanida, Nano Lett. **10**, 414–419 (2010)
6. Y.G. Lu, S.N. Song, Z.T. Song, B. Liu, J. Appl. Phys. **109**, 064503 (2011)
7. H. Zou, X. Zhu, Y. Hu, Y. Sui, W. Wu, J. Xue, L. Zheng, Z. Song, CrystEngComm **18**, 6365–6369 (2016)
8. Y. Hu, H. Zou, J. Zhang, J. Xue, Y. Sui, W. Wu, L. Yuan, X. Zhu, S. Song, Z. Song, Appl. Phys. Lett. **107**, 263105 (2015)
9. M. Putero, M.-V. Coulet, T. Ouled-Khachroum, C. Muller, C. Baehtz, S. Raoux, APL Mater. **1**, 062101 (2013)
10. C. Cabral Jr., L. Krusin-Elbaum, J. Bruley, S. Raoux, V. Deline, A. Madan, T. Pinto, Appl. Phys. Lett. **93**, 071906 (2008)
11. F. Rao, Z.T. Song, K. Ren, X.L. Li, L.C. Wu, W. Xi, B. Liu, Appl. Phys. Lett. **95**, 032105 (2009)

12. T.C. Chong, L.P. Shi, R. Zhao, P.K. Tan, J.M. Li, H.K. Lee, X.S. Miao, A.Y. Du, C.H. Tung, Appl. Phys. Lett. **88**, 112114 (2006)
13. C.C. Tan, L. Shi, R. Zhao, Q. Guo, Y. Li, Y. Yang, T.C. Chong, J.A. Malen, W.-L. Ong, T.E. Schlesinger, J.A. Bain, Appl. Phys. Lett. **103**, 133507 (2013)
14. R.E. Simpson, P. Fons, A.V. Kolobov, T. Fukaya, M. Krbal, T. Yagi, J. Tominaga, Nat. Nanotechnol. **6**, 501–505 (2011)
15. M. Putero, M.-V. Coulet, T. Ouled-Khachroum, C. Muller, C. Baehtz, S. Raoux, Appl. Phys. Lett. **103**, 231912 (2013)
16. T.H. Jeong, M.R. Kim, H. Seo, S.J. Kim, S.Y. Kim, J. Appl. Phys. **86**, 774 (1999)
17. T.C. Chong, L.P. Shi, X.Q. Wei, R. Zhao, H.K. Lee, P. Yang, A.Y. Du, Phys. Rev. Lett. **100**, 136101 (2008)
18. Y. Hu, J. Zhai, H. Zeng, S. Song, Z. Song, J. Appl. Phys. **117**, 175704 (2015)
19. X. Ji, L. Wu, W. Zhou, M. Zhu, F. Rao, Z. Song, L. Cao, S. Feng, Appl. Phys. Lett. **106**, 023118 (2015)
20. T. Morikawa, K. Kurotsuchi, Y. Fujisaki, Y. Matsui, N. Takaura, Jpn. J. Appl. Phys. **51**, 031201 (2012)
21. H.-Y. Cheng, S. Raoux, J.L. Jordan-Sweet, J. Appl. Phys. **115**, 093101 (2014)
22. X. Wei, T. Luping, T.T. Chong, T. Rong, T.H. Koon, Jpn. J. Appl. Phys. **46**, 2211–2214 (2007)
23. H.K. Peng, K. Cil, A. Gokirmak, G. Bakan, Y. Zhu, C.S. Lai, C.H. Lam, H. Silva, Thin Solid Films **520**, 2976–2978 (2012)
24. F. Wei, L. Wang, T. Kong, L. Shi, R. Huang, J. Zhang, G. Cheng, Appl. Phys. Lett. **103**, 181908 (2013)
25. J. Zhou, Y. Chen, W. Zhou, X. Miao, N. Yu, H. Liu, T. Lan, J. Yan, Appl. Surf. Sci. **280**, 862–867 (2013)
26. Y. Hu, S. Li, T. Lai, S. Song, Z. Song, J. Zhai, J. Alloys Compd. **581**, 515–518 (2013)
27. M.C. Sun, B. Shen, C.Z. Wang, S.N. Song, Z.T. Song, J.W. Zhai, Electrochem. Solid State Lett. **15**, H115–H117 (2012)
28. Y.F. Hu, X.Y. Feng, S.M. Li, T.S. Lai, S.N. Song, Z.T. Song, J.W. Zhai, Scr. Mater. **93**, 4–7 (2014)